ABSTRACT OF THE DISCLOSURE

The image processing apparatus comprises an input I/F memory which reads pixels having a predetermined length, subjects the read pixels to buffering, and writes them in a SIMD type processor. The SIMD type processor performs batch processing of the pixels. Further, an output I/F memory reads the pixels batch-processed by the SIMD type processor, subjects the read pixels to buffering and writes them in a predetermined output destination. Read and/or write timing of IN_FIFO and OUT_FIFO is appropriately controlled.